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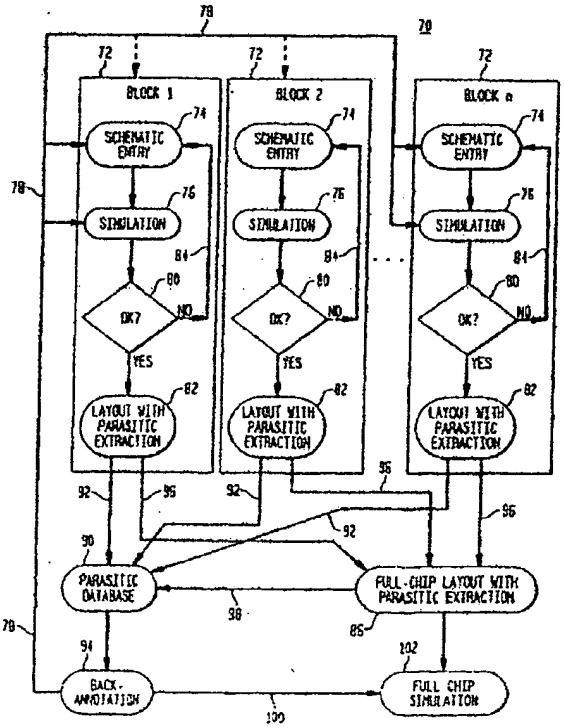
(54) Title: METHOD FOR DESIGN AND LAYOUT OF INTEGRATED CIRCUITS



(57) Abstract: A method, which improves the design, layout, and performance of a very large scale integrated circuit (VLSI) having a plurality of blocks and having parasitic elements, includes initially designing each of the blocks in separate parallel efforts; initially simulating each block design; and making extractions of parasitic elements identified in each block and storing the information thus obtained in a database common to all blocks. The method further includes back annotating the parasitic extractions on a continual basis to each of the blocks to benefit the initial design, simulation, and subsequent steps; making a layout with parasitic extractions for each block design after successful simulation thereof; making a full chip layout with parasitic extraction; and simulating with back annotation of parasitic elements the full chip layout to optimize the design thereof.

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METHOD FOR DESIGN AND LAYOUT OF INTEGRATED CIRCUITS

Field of the Invention

This invention relates to a method for improving the design and layout processes for integrated circuits, particularly very large scale integrated circuits.

Background of the Invention

Spurred by the increasing application of integrated circuits (ICs) to numerous new and different uses, ICs are becoming more and more complex, some with hundreds of millions of devices on a single small semiconductor chip. This in turn has made the design and layout of very large scale integrated circuits (VLSIs) far more complex and time consuming than the much simpler ICs in the past. Because of the great expense in putting a VLSI into production and to obtain even a few actual operating units for testing, the design and layout processes currently being used rely on computer-aided-design and computer simulation to evaluate the expected performance of an actual unit.

The design of VLSI circuits consists of three major steps. In the first step circuit schematics are created by designers. The next step confirms the correct logical behavior and timing by analog, digital or mixed signal simulation. Usually these two steps are iterated many times, before the layout work, which is the third step, starts.

One of the biggest problems for today's sub-micron VLSI designs is that the influence of parasitic elements, such as resistance and capacitance of wires (i.e., circuit traces), becomes more and more important and has to be taken seriously into account.

A signal in a path is delayed by the internal delay associated with a logic gate delay, denoted as a "gate delay" in its path and by the delay, denoted as the "wire delay", associated with the electrical connector (wire) used to carry the signal. In older, less dense, e.g., .35 micron designed ICs, technology, signal delay is dominated by the gate-delay, which is approximately 80% of the total delay for a typical path. This situation changes dramatically with higher density integration. For high-density, e.g., .18 micron designed intergrated circuits, technology, signal delay is dominated by the wire delay, which is about 70% of the total delay. This shows that it is very important to calculate the parasitic elements and enter these into the simulations as early as possible. Usually parasitic elements (e.g., for bus lines) have been estimated by the designers and included in the schematics. However, this method is limited, because it is not possible to take all parasitic elements into account on a current basis as the layout is being made. After the layout step, it is then possible to extract the parasitic elements from the layout data and include these in the simulations (Back-Annotation). A major problem of such a design flow is to maintain the consistency between the design and the parasitic database.

A VLSI such as a high-density, high speed dynamic random access memory (DRAM), may be divided into a plurality of blocks or sub-divisions to improve operating efficiency. The blocks are intended to operate simultaneously and independently of each other. But because of the dense spacings of the blocks and very short signal pulse rise times (e.g., 20 picoseconds or so), particular care must be taken to minimize the ill effects of parasitic

conditions since otherwise the operation of one block may adversely affect the operation and timing of another block and the DRAM will not operate with best efficiency or optimum speed. The present invention addresses this problem.

Summary of the Invention

In accordance with the present invention, in one embodiment thereof, there is provided an improved method for the design and layout of integrated circuits, particularly very large scale integrated circuits (VLSIs) such as high-density, high speed dynamic random access memories (DRAMs) having a plurality of blocks for increased efficiency of operation. The blocks are designed and laid out separately, using computer-aided-design and computer simulation, and are then combined into an overall chip layout. An integral part of the computer-aided-design and simulation process is simultaneous identification of parasitic elements being generated during layout. During design and layout of each block, parasitic elements are recognized and from these elements parasitic extractions (i.e., calculated values of the parasitic elements in each block) are provided for all blocks on an immediate and continuing basis. These parasitic extractions are immediately provided, both on an initial and on an ongoing basis, to a centralized database. Thus the design and layout of each block and of all the blocks combined together, benefit from the combined information immediately available regarding all parasitic elements. As a result the total time for the design, layout, and computer simulation of the overall chip is lessened, and the speed and operation of the chip are optimized.

Viewed from a first method aspect, the present is directed to a method for design and layout of an integrated circuit having

parasitic elements. The method comprising the steps of: making initial designs of various portions of the integrated circuit; evaluating the designs by computer simulations; making extractions of parasitic elements as soon as available in the initial design and simulation steps and storing such extractions in a database common to all portions of the integrated circuit; back annotating the information stored in the database on an ongoing basis to benefit immediately the initial design and simulation, and subsequent steps; making layouts with parasitic extractions of the various portions of the integrated circuit before and after successful simulations; and making a full chip layout of the integrated circuit with parasitic extractions and simulating same.

Viewed from a second method aspect, the present is directed to a method for design and layout of a very large scale integrated circuit (VLSI) having a plurality of blocks and having parasitic elements. The method comprises the steps of: initially designing each of the blocks in separate parallel efforts; initially simulating each block design; simultaneously making extractions of parasitic elements identified in each block and storing the information thus obtained in a database common to all blocks; back annotating the parasitic extractions on a continual basis to each of the blocks to benefit the initial design, simulation, and subsequent steps; making a layout with parasitic extractions for each block design after successful simulation thereof; making a full chip layout with parasitic extraction; and simulating with back annotation of parasitic elements the full chip layout to optimize the design thereof.

Viewed from a third method aspect, the present is directed to a method for design and layout of a very large scale integrated circuit (VLSI), including a dynamic random access memory (DRAM) having widths less than about 0.2 micron and having parasitic elements which can significantly affect signal timings. The method comprises the steps of: making initial designs of various portions of the VLSI; evaluating the designs by computer simulations; making extractions of parasitic elements as part of the initial design and simulation steps and storing such extractions in a database common to all portions of the VLSI; back annotating the information stored in the database on an ongoing basis to optimize the initial design, simulation, and subsequent steps and to minimize the effects of parasitic elements; making layouts with parasitic extractions of the various portions of the VLSI after successful simulations; and making a full chip layout of the VLSI with parasitic extractions and simulating same such that the operation of the VLSI is optimized.

Viewed from a fourth method aspect, the present invention is directed to a method for design and layout of a dynamic random access memory (DRAM) having a plurality of blocks and having parasitic elements which can affect signal timings. The method comprises the steps of: initially designing each of the blocks in separate parallel efforts; initially simulating each block design; making extractions of parasitic elements identified in each block and storing the information thus obtained in a database common to all blocks; back annotating the parasitic extractions on a continual basis to each of the blocks to optimize the initial design, simulation, and subsequent steps and to minimize the effects of parasitic elements; making a layout with parasitic extractions for

each block design after successful simulation thereof; making a full chip layout with parasitic extraction; and simulating with back annotation of parasitic elements the full chip layout to optimize the design thereof.

Viewed from a fourth method aspect, the present invention is directed to a method for design and layout of very large scale integrated circuit (VLSI), including high-density dynamic random access memories each having a plurality of blocks and having signal delay dominated by wire delay instead of gate delay. The method comprises the steps of: initially designing blocks in separate efforts; initially simulating each block design; making extractions of parasitic elements block-by-block on an ongoing basis and storing the extractions in a database common to all blocks; back annotating the parasitic extractions on an ongoing basis to each of the blocks to benefit initial design, simulation, and subsequent steps; repeating the initial design and simulation steps in a block if a shortcoming is discovered; making a layout with parasitic extractions for each block design after successful simulation thereof; making a full chip layout with parasitic extraction; and simulating with back annotation of parasitic elements the full chip layout to minimize the effects of parasitic elements on operation of the VLSI.

Viewed from an apparatus aspect, the present invention is directed to an improved integrated circuit or very large scale integrated circuit, including a dynamic random access memory, made in accordance with any of the above described methods.

A better appreciation of the invention together with a fuller appreciation of its many advantages will best be gained from the

following description given in conjunction with the accompanying drawings and claims.

Brief Description of the Drawings

FIG. 1 is a schematic representation of a prior art method for design and layout, and computer simulation of a very large scale integrated circuit (VLSI) having a plurality of circuit blocks;

FIG. 2A is a schematic representation of an enlarged part of the circuit of FIG. 1 illustrating parasitic resistance and capacitance in the layout;

FIG. 2B is a schematic illustration of the relative size of parasitic capacitance coupling from one layer of the circuit of FIG. 2A to an adjacent layer of the circuit;

FIG. 3A is a schematic representation of the circuit of FIG. 2A showing a change in a wire layout on one layer of the circuit;

FIG. 3B is a schematic illustration of the relative size of parasitic capacitance coupling from one layer of the circuit of FIG. 3A to an adjacent layer of the circuit, the parasitic capacitance here being relatively larger than that illustrated in FIG. 2B; and

FIG. 4 is a schematic representation of a method, provided in accordance with the present invention, for design and layout, and computer simulation of a VLSI having a plurality of circuit blocks.

Detailed Description

Referring now to FIG. 1, there is shown a schematic diagram 10 of a prior-art method for computer-aided-design, layout, and computer simulation of a very large scale integrated circuit (VLSI) having a plurality of circuit blocks 12 (respectively identified as "A", "B", to "n" and which are to be integrated on an overall

circuit chip, not shown here. The design flow indicated by the diagram 10 starts with a first step for each respective block 12 of entering a schematic circuit diagram for the block, as indicated by a respective box 14 titled "schematic entry". Then the designer or designers of each block 12 (i.e., A, B,...n) evaluate the respective circuits represented by the blocks 12 by using a computer (not shown) to simulate the circuit-logic and timing, as indicated by a box 16 titled "SIMULATION". If the design appears satisfactory, as indicated by a box 18 titled "OK", the design proceeds to a layout stage, indicated by a respective box 20. If, on the other hand, a design shortcoming is uncovered by the simulation at the box 16, the design is modified and reentered as indicated by a return line 22 from the box 18 to the box 14.

Once the layout of individual blocks 12 has been satisfactorily completed, the design proceeds to the overall circuit layout of all the blocks 12 (A, B,...n) on an entire chip, as indicated by the box 24 (Full Chip layout). After the full chip layout is completed parasitic extraction (indicated by a box 26) for the entire circuit is carried out by computer calculation of values of parasitic capacitances and resistances. These values are then entered into a parasitic database, indicated by a box 28. Up to this point in the overall design and layout process, as represented by the schematic diagram 10, there has been no effective way in this prior-art method to take into account the parasitic elements and their cumulative effects on the operation of the full chip circuit. As will be explained in greater detail hereinafter, parasitic elements can have important and adverse effects on the operations of the individual blocks 12, and on the performance, and speed of the

full chip circuit. Except perhaps for a local effort, indicated by a dashed-line box 30 (parasitic extraction), a dashed line box 32 (local database), and a dashed line box 34 (back annotation) shown adjacent the block 12(A) and made by the engineer-designer laying out that particular block, there is no overall way provided in the diagram 10 for the designers of the various blocks 12 to take into account, prior to the full chip layout of box 24, the combined and interrelated effects of parasitic elements. This is a serious limitation of the method and causes difficulties in subsequently optimizing the operation and timing of the full chip circuit, as well as the respective blocks themselves.

After being entered in the parasitic database, (box 28), the parasitic values are used in conjunction with the full chip layout (box 24) in a "back annotation" step, indicated by a box 36, to modify the design and/or layout of the full chip so that a full-chip computer simulation, indicated by a box 38, can be made. Needed modifications or changes indicated by the simulation are than referenced back to the beginning of each respective block 12, as indicated by a dashed line 39, and the design process with changes, is repeated. Such design process is iterated as many times as deemed necessary to optimize the performance of the full chip.

Referring now to FIG. 2A, there is shown an enlarged schematic representation in plan view, of a small part of a VLSI circuit 40 on a semiconductor chip 42 (shown in dashed outline). The circuit 40 has a lower insulating layer 44 (only a portion of which is shown) containing a circuit trace or "wire" 46 connecting a point "A" to a point "B". Lying on top of the layer 44 and its wire 46 is an insulation layer 48 (only a portion of which is shown) containing a

wire 50 which is shown cross-hatched to indicate it lies on a level higher than the wire 46. Where the wire 50 crosses above the wire 46, in a region indicated by a small circle 52, there is some parasitic capacitance between the two wires.

Referring to FIG. 2B, there is shown, connected between the wire 46 and the wire 50, a capacitor 54 representing the parasitic capacitance between the wires in the region 52 (FIG 2A). Depending on the size of the parasitic capacitor 54, the operation of that portion of the VLSI circuit 40 on the layer 44 will affect to a greater or smaller degree that portion of the circuit 40 on the upper layer 48. During the design and layout of the respective blocks 12 (FIG. 1) it is evident that many parasitic elements, such as the parasitic resistances and capacitances of the wires 46 and 50, are created, and quite possibly changed in different, uncoordinated ways. Thus, an engineer in the course of laying out a respective block 12 (e.g., block A) may decide that a wire, such as the wire 50, which happens to be in his layout of that block has too much parasitic resistance. The engineer may then change the configuration of that wire to lower its resistance, though this change also affects an adjacent block 12 (e.g., block B). Such layout changes can result in significant and unforeseen changes in the operations of the blocks 12, and in the overall operation of the full VLSI circuit 40.

Referring now to FIG. 3A, there is shown a schematic circuit 56, which is closely similar to the circuit 40 (FIG. 2A). The circuit 56 however has an upper wire 58 reconfigured from the wire 50 (FIG. 2A) to lower the parasitic resistance of the wire 50 by making the wire 58 substantially wider. However, as indicated by an

oval area 60, the parasitic capacitance here between the wires 46 and 58 is substantially higher than the parasitic capacitance between the wires 46 and 50 as indicated by the small circle 52 in FIG. 2A.

Referring now to FIG. 3B, there is shown connected between the wire 46 and the wire 58, a capacitor 62 representing the parasitic capacitance between the wires in the oval area 60 (FIG. 3A). As pointed out above, because the oval area 60 is much larger than the area of the region 52 (FIG. 2A), the capacitor 62 will be substantially larger than the capacitor 54. This in turn further increases the delay of a signal on the wire 46 in going from point A to point B in the circuit 56 of FIG. 3A. The illustrations given in FIGs. 2A, 2B, 3A, and 3B highlight the problems caused by parasitic elements, and of changes thereof made during a prior-art design and layout process of a VLSI as schematically shown by the diagram 10.

Referring now to FIG. 4, there is shown a schematic diagram 70 of a method, provided in accordance with the present invention, for computer-aided-design, layout, and computer simulation of a very large scale integrated circuit (VLSI) having a plurality of circuit blocks 72 (respectively identified as Block "1", Block "2", ...Block "n", and which are to be integrated to form an integrated circuit (IC, not shown here). A VLSI is a type of integrated circuit (IC). The design flow indicated by the diagram 70 starts with a first step for each block 72 of entering a schematic circuit diagram of that block, as indicated by a respective box 74 titled "SCHEMATIC ENTRY". Then the designer or designers of each block 72 (i.e., BLOCK 1, 2, ...n) evaluate the respective circuits represented by the blocks 72 by using a computer (not shown) to simulate the

circuit-logic and timing as indicated by a respective box 76 titled "SIMULATION". During these initial steps and simultaneous with them, "back annotation" of values of parasitic elements, which values have become available in the various blocks 72 during the overall design process as it progresses in any or all of the blocks 72, is immediately provided by an information feedback loop indicated by a common lead 78 connected to the boxes 74 and 76 in each of the blocks 72. This continual and global feedback of information regarding parasitic elements will be explained in greater detail hereinafter. Such information provided in the earliest stages of design is of great importance and value to the success of the overall method as illustrated by the diagram 70.

If after the "SIMULATION" step, indicated by the box 76, the design appears satisfactory, as indicated by the "YES" output of a box 80 ("OK"), the design proceeds to a block layout stage, as indicated by a box 82 titled "LAYOUT WITH PARASITIC EXTRACTION". Thus even before full chip layout, block layout has the benefit of parasitic extraction. If a design shortcoming is uncovered by the simulation at the box 76, i.e., the "NO" output of box 80, the design is modified and reentered as indicated by a return line 84 from the box 80 to the box 74. Simultaneously, any changes in parasitic extractions previously made in a respective block 72 are fed back via the loop 78 into the design process.

Before the step of making a full chip layout, indicated by a box 86 titled "FULL CHIP LAYOUT WITH PARASITIC EXTRACTION", information regarding the parasitic elements in all of the blocks 72 has been fed into a common or global parasitic database (box 90) as indicated by the arrows 92 from the blocks 72. All such parasitic

extractions (and any changes therein) from a respective block 72 are simultaneously fed from the database 90 via a step of "back annotation" (box 94) to the feedback loop 78, and thence immediately to the individual blocks 72, as was explained above. Thus even before a full layout is made, those designing and laying out the respective blocks 72 have the benefit of knowing what parasitic elements exist and which may inadvertently or adversely affect the performance of the blocks themselves or of the overall VLSI. The designers, operating according to the new method of diagram 70 provided by the invention, are able at the earliest stages of design and layout, to avoid or to minimize the effects of parasitic elements. Thus inadvertent creation of a large parasitic capacitance in an uncoordinated attempt to lower parasitic resistance, as illustrated by FIGs. 2A, 2B, 3A, and 3B, is easily avoided before it even occurs.

The layout (box 82) of each individual block 72 is combined into a full chip layout (box 86), as is indicated by the arrows 96. Parasitic extraction from the full chip layout (box 86) is also applied to the parasitic database 90, as indicated by an arrow 98, so that back annotation (box 94) of all parasitic extractions can be applied, as is indicated by an arrow 100 to the final step of full chip simulation (box 102). The providing of information on all parasitic elements as soon as known, and well before full chip simulation, greatly aids the optimizing of a VLSI and its component blocks. This also considerably shortens the time required by the engineers in doing or re-doing the various steps of design, layout and full chip simulation of the VLSI.

The above description is intended in illustration and not in limitation of the invention. Various changes and modifications in the method illustrated may occur to those skilled in the art and may be made without departing from the spirit and scope of the invention as set forth in the accompanying claims. In particular, the invention is not limited to a particular size or kind of VLSI or to one having a particular number of blocks, nor is the invention limited to the exact sequence and number of steps set forth.

What is claimed is:

1. A method for design and layout of an integrated circuit having parasitic elements, the method comprising the steps of:

making initial designs of various portions of the integrated circuit;

evaluating the designs by computer simulations;

making extractions of parasitic elements as soon as available in the initial design and simulation steps and storing such extractions in a database common to all portions of the integrated circuit;

back annotating the information stored in the database on an ongoing basis to immediately benefit the initial design and simulation, and subsequent steps;

making layouts with parasitic extractions of the various portions of the integrated circuit before and after successful simulations; and

making a full chip layout of the integrated circuit with parasitic extractions and simulating same.

2. A method for design and layout of a very large scale integrated circuit (VLSI) having a plurality of blocks and having parasitic elements, the method comprising the steps of:

initially designing each of the blocks in separate parallel efforts;

initially simulating each block design;

simultaneously making extractions of parasitic elements identified in each block and storing the information thus obtained in a database common to all blocks;

back annotating the parasitic extractions on a continual basis to each of the blocks to benefit the initial design, simulation, and subsequent steps;

making a layout with parasitic extractions for each block design after successful simulation thereof;

making a full chip layout with parasitic extraction; and

simulating with back annotation of parasitic elements the full chip layout to optimize the design thereof.

3. The method of claim 2 wherein parasitic extractions are also made from the full chip layout, and back annotation with all extractions stored in the database is applied to the step of simulating the full chip layout.

4. An improved VLSI made according to the method of claim 2.

5. A method for design and layout of a very large scale integrated circuit (VLSI), including a dynamic random access memory (DRAM) having widths less than about 0.2 micron and having parasitic elements which can significantly affect signal timings, the method comprising the steps of:

making initial designs of various portions of the VLSI;

evaluating the designs by computer simulations;

making extractions of parasitic elements as part of the initial design and simulation steps and storing such extractions in a database common to all portions of the VLSI;

back annotating the information stored in the database on an ongoing basis to optimize the initial design, simulation, and subsequent steps and to minimize the effects of parasitic elements;

making layouts with parasitic extractions of the various portions of the VLSI after successful simulations; and

making a full chip layout of the VLSI with parasitic extractions and simulating same such that the operation of the VLSI is optimized.

6. A method for design and layout of a dynamic random access memory (DRAM) having a plurality of blocks and having parasitic elements which can affect signal timings, the method comprising the steps of:

initially designing each of the blocks in separate parallel efforts;

initially simulating each block design;

making extractions of parasitic elements identified in each block and storing the information thus obtained in a database common to all blocks;

back annotating the parasitic extractions on a continual basis to each of the blocks to optimize the initial design, simulation, and subsequent steps and to minimize the effects of parasitic elements;

making a layout with parasitic extractions for each block design after successful simulation thereof;

making a full chip layout with parasitic extraction; and

simulating with back annotation of parasitic elements the full chip layout to optimize the design thereof.

7. The method of claim 6 wherein parasitic extractions are also made from the full chip layout, and back annotation with all extractions stored in the database is applied to the step of simulating the full chip layout.

8. The method of claim 6 wherein the DRAM has widths smaller than about 0.2 micron and signal timing is dominated by wire delay rather than gate delay.

9. An improved DRAM made according to the method of claim 6.

10. A method for design and layout of very large scale integrated circuit (VLSI), including high-density dynamic random access memories each having a plurality of blocks and having signal delay dominated by wire delay instead of gate delay, the method comprising the steps of:

initially designing blocks in separate efforts;

initially simulating each block design;

making extractions of parasitic elements block-by-block on an ongoing basis and storing the extractions in a database common to all blocks;

back annotating the parasitic extractions on an ongoing basis to each of the blocks to benefit initial design, simulation, and subsequent steps;

repeating the initial design and simulation steps in a block if a shortcoming is discovered;

making a layout with parasitic extractions for each block design after successful simulation thereof;

making a full chip layout with parasitic extraction; and

simulating with back annotation of parasitic elements the full chip layout to minimize the effects of parasitic elements on operation of the VLSI.

FIG. 1
(PRIOR ART)

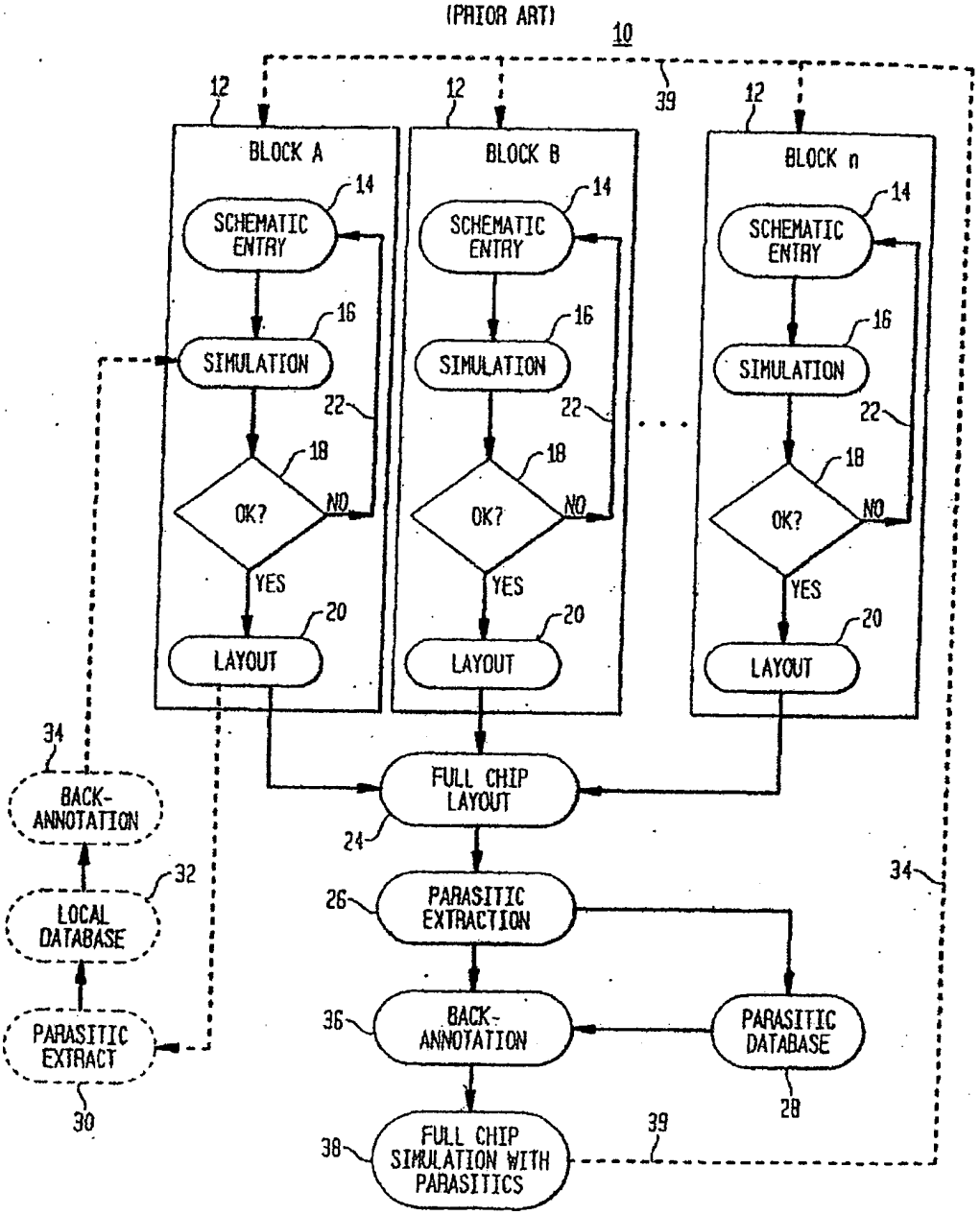


FIG. 2A

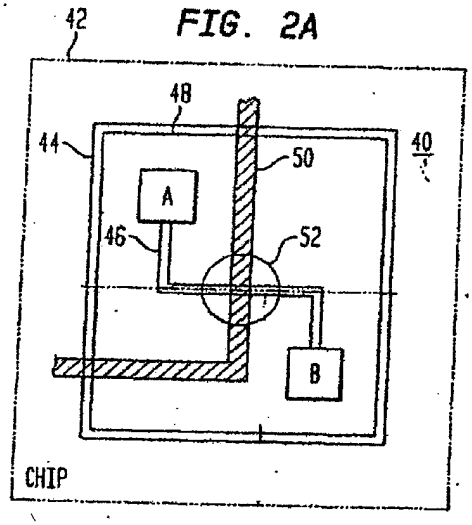


FIG. 3A

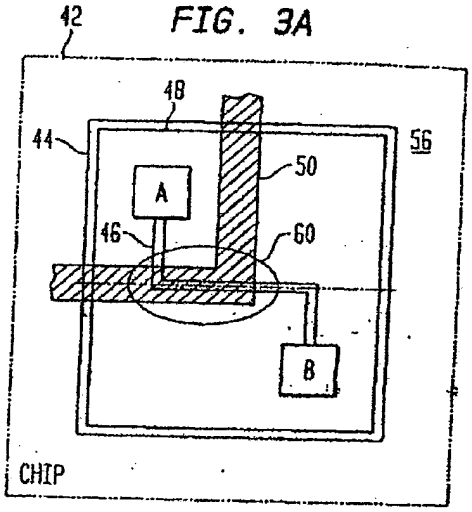


FIG. 2B

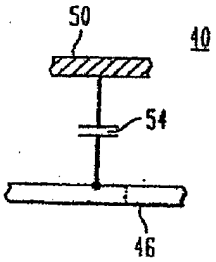


FIG. 3B

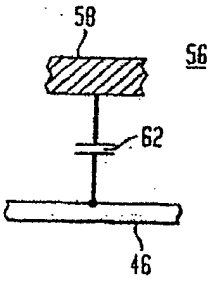
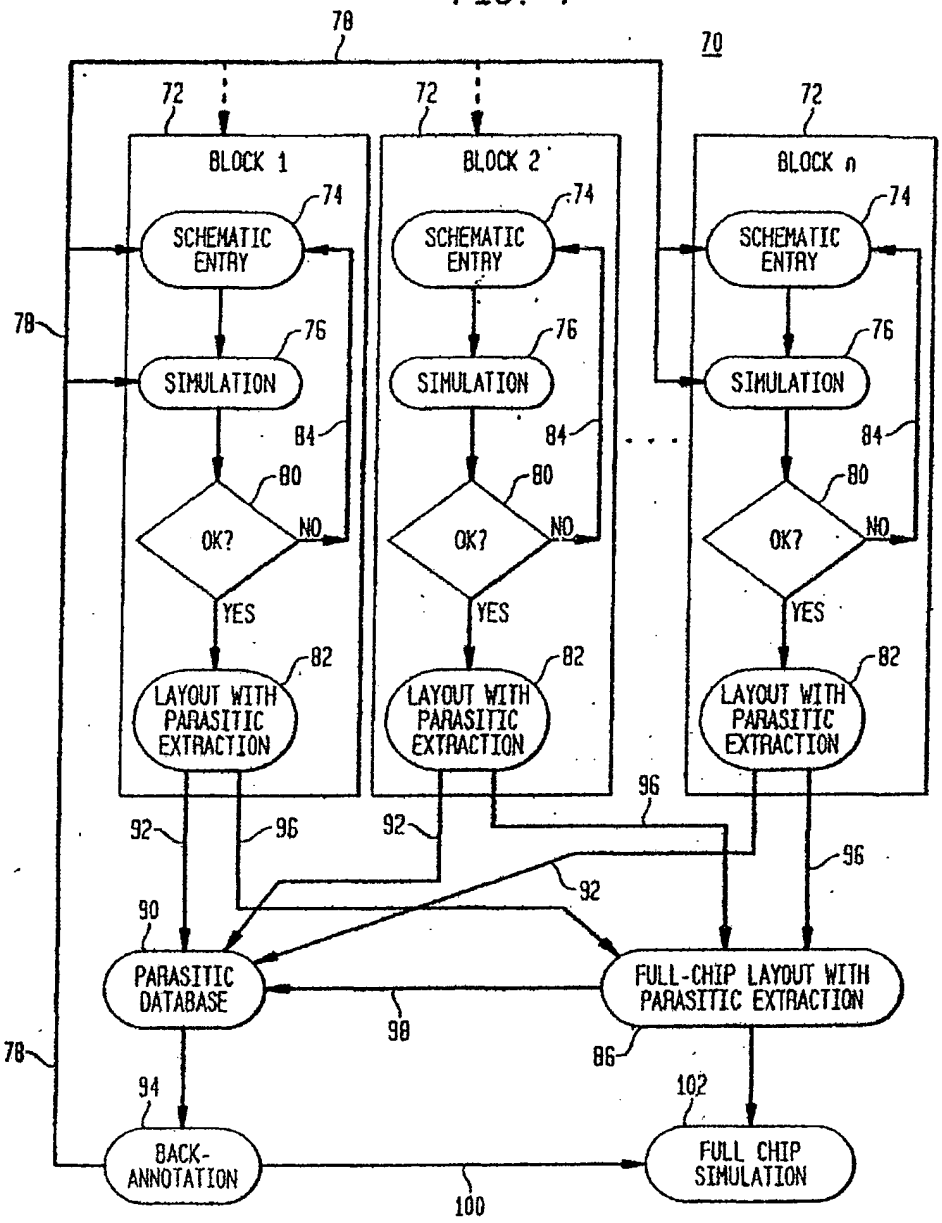


FIG. 4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LAYOUT WITH PARASITIC EXTRACTION
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96
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PARASITIC DATABASE
98
FULL-CHIP LAYOUT WITH PARASITIC EXTRACTION
86
94
BACK-ANNOTATION
100
102
FULL CHIP SIMULATION